WHAT IS CLAIMED IS:

1. An error rate determining method for determining an error rate of a semiconductor memory device implementing detection and correction of an error existing in a plurality of pieces of data stored in said semiconductor memory device by using said pieces of data and inspection bits provided for said pieces of data, said error rate determining method comprising the steps of:

cumulatively adding a first value to a total in the event of a detected first detection signal indicating non-existence of an error in said pieces of data;

subtracting a second value greater than said first value from said total in the event of a detected second detection signal indicating existence of an error in said pieces of data; and

determining said error rate on the basis of a value of said total.

2. An error rate determining method according to claim 1, whereby said pieces of data and said inspection bits are read out from a memory circuit.

3. A semiconductor integrated circuit device comprising:

a memory circuit comprising dynamic memory cells each

comprising a storage capacitor and an address selection MOSFET, and provided with an information sustaining mode; and

a data holding control circuit comprising an additional memory circuit, an ECC circuit and an error rate setting circuit,

wherein said ECC circuit operates in said information sustaining mode to carry out a first operation of reading out a plurality of pieces of data from said memory circuit, generating inspection bits for detection and correction of an error existing in said pieces of data and storing said inspection bits into said additional memory circuit and to carry out a second operation of reading out said pieces of data from said memory circuit, reading out said inspection bits from said additional memory circuit and detecting and correcting an error existing in said pieces of data,

wherein said error rate setting circuit carries out an error rate monitoring operation of adding a first value according to a first detection signal indicating non-existence of an error detected by said ECC circuit to the total value and subtracting a second value according to a second detection signal indicating existence of an error detected by said ECC circuit from the total value, said second value being larger than said first value, and

wherein said error rate setting circuit carries out an

error rate setting operation of changing a refresh cycle according to said total value.

4. A semiconductor integrated circuit device according to claim 3, wherein said additional memory circuit comprises dynamic memory cells in a configuration identical with that of said memory circuit and shares an X-system address select circuit with said memory circuit.

5. A semiconductor integrated circuit device according to claim 3, wherein:

there is provided a refresh address generating circuit shared by refresh operations carried out in said information sustaining mode and in a normal mode including operations to read out and write data from and into said memory circuit;

said ECC circuit is provided with an ECC address generating circuit for selecting said pieces of data from word lines specified by a refresh address; and

an X-system address signal generated by said refresh address generating circuit and a Y-system address signal generated by said ECC address generating circuit are supplied to an address control circuit and supplied to said memory circuit in said information sustaining mode and in said normal mode.

6. A semiconductor integrated circuit device according to claim 5, wherein:

said refresh address generating circuit generates an oscillation signal with the frequency thereof controlled by a temperature-dependent timer and a refresh address signal output by counting the number of activation signals produced by a variable divider circuit that divides the frequency of said oscillation signal; and

said error rate select circuit sets a dividing ratio of said variable divider circuit to change said refresh period to a value proper for an error rate.

7. A semiconductor integrated circuit device according to any one of claims 3 to 6, wherein a ratio of said first value to said second value is set at a value appropriate for an allowable error rate.

8. A semiconductor integrated circuit device according to claim 7, wherein:

said allowable error rate is determined from a binary number consisting of a plurality of bits;

said first detection signals are supplied to a first binary counter for said bits to be counted by said first binary

counter and a carry signal generated by said first binary counter is supplied to a second binary counter which carries out a counting-up operation in response to said supplied carry;

said second detection signal is supplied to said second binary counter which carries out a counting-down operation in response said supplied second detection signal; and

a count value produced by said second binary counter is used as a dividing ratio of said variable divider circuit.

9. A semiconductor integrated circuit device according to claim 3, wherein said memory circuit and said data holding control circuit are formed on a single semiconductor chip.

10. A semiconductor integrated circuit device according to claim 3, wherein said memory circuit is formed on a first semiconductor chip, said data holding control circuit is formed on a second semiconductor chip and said first as well as second semiconductor chips are mounted on a multichip package.

11. A semiconductor integrated circuit device according to claim 10, wherein:

said first and second semiconductor chips are connected

to each other by a control command and data communication line; and

a communication circuit is provided in each of said first and second semiconductor chips.

12. A semiconductor integrated circuit device according to claim 10, wherein said first and second semiconductor chips are mounted on a single package in a layered structure.

13. A semiconductor integrated circuit device according to claim 3 wherein said data holding control circuit is provided with a function for controlling a substrate voltage or the level of a voltage for writing data into memory cells in accordance with a cumulative quantity computed in said error rate monitoring operation.